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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,984	12/28/2001	Yong Jin Cho	8733.563.00	3746

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MCKENNA LONG & ALDRIDGE LLP
1900 K STREET, NW
WASHINGTON, DC 20006

EXAMINER	
DI GRAZIO, JEANNE A	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 11/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,984	CHO ET AL.	
	Examiner	Art Unit	
	Jeanne A. Di Grazio	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *June & Aug. 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims

Claims 1-12 are pending. Claims 1, 3 and 8 have been amended per Amendment of August 25, 2004.

Priority

Priority to Korean Patent Application No. P2001-024581 (May 7, 2001) is claimed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors.

In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US 6,580,473 B2) in view of Song et al. (US 5,886,757) and further in view of Ono et al. (US 5,760,854).

Per claims 1 (amended) and 3 (amended): Kim teaches and discloses an active matrix display device with ladder-shaped electrodes or pixel electrode contacting a side of a drain electrode (Title, entire patent). With reference to Figures 8 and 9, Kim has a drain electrode (170) that is electrically connected to a pixel electrode (7) through a contact hole. Kim has a contact hole (not numbered) in Figures 8 and 9 that is formed over part of the drain electrode (170) and also formed over part of a pixel region.

Kim does not appear to explicitly call out a plurality of gate lines, a plurality of data lines, and a plurality of TFTs, the gate lines crossing the data lines to define a pixel region and the TFTs being formed at crossing points of the gate and data lines.

Song teaches and discloses a liquid crystal display device and method for fabricating the device (Title, entire patent). Song notes, in the Background of the Invention, that a conventional LCD device has (referring to Figure 1 prior art) a plurality of gate lines (1), a plurality of data lines (2) crossing the gate lines (1), a plurality of TFTs (5) formed at the cross-over points of the gate (1) and data (2) lines and a plurality of pixel electrodes (3) connected to the TFTs (5) (Column 1, Lines 34-46). Song also notes that the conventional LCD device has gate lines (1) crossing data lines (2) to define a pixel region and in each pixel region the TFT (5) and pixel electrode (3) are disposed (Id.).

One of ordinary skill in the art of liquid crystals would have had the reason, suggestion, and motivation to include a plurality of gate lines, a plurality of data lines, and a plurality of TFTs, the gate lines crossing the data lines to define a pixel region and the TFTs being formed at crossing points of the gate and data lines into an active matrix display because one of ordinary skill in the art would recognize these elements as essential elements in a functional liquid crystal display device and to drive the liquid crystal display device.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Kim in view of Song to include a plurality of gate lines, a plurality of data lines, and a plurality of TFTs, the gate lines crossing the data lines to define a pixel region and the TFTs being formed at crossing points of the gate and data lines into an active matrix display as essential elements in a functional liquid crystal display device and for driving the liquid crystal display device.

Kim does not appear to explicitly specify *wherein the pixel electrode directly contacts the insulating substrate*.

Ono teaches and discloses a liquid crystal display apparatus wherein a pixel electrode is made to directly contact a substrate (Column 2, Lines 30-34). Such a configuration reduces the number of manufacturing steps and contributes to a high yield and furthermore contributes to a bright image display (Column 2, Lines 10-17).

Ono is evidence that ordinary workers in the field of liquid crystal would have found the reason, suggestion and motivation to have a pixel electrode directly contact a substrate to (1) reduce the number of manufacturing steps in the manufacturing process for the device, (2) to improve the yield and (3) to contribute to a bright image display.

Therefore, it would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made to modify Kim in view of Ono to (1) reduce the number of manufacturing steps in the manufacturing process for the device, (2) to improve the yield and (3) to contribute to a bright image display.

As to claim 2, Kim has (Figures 8 and 9) a gate line (130a) formed on an insulating substrate (100), a gate insulating layer (120) formed on an entire surface of the insulating substrate (100) including the gate line (130a), an amorphous silicon active region (110) and an ohmic contact layer (not shown but described at Column 7, Lines 36-61) sequentially deposited at a predetermined portion on the gate insulating layer (120), source (150) and drain (170) electrodes formed right and left of the ohmic contact layer, a passivation film (160) formed on the entire surface of the substrate (100) including the source (150) and drain (170) electrodes, a contact hole (not numbered), and pixel electrode (7) formed on the passivation film (160) and the contact hole.

As to claims 4, 6, and 7, the contact hole of Kim is formed over an edge part of the drain electrode (170) and the pixel region adjacent to the edge part of the drain electrode (170)(Figures 8 and 9).

As to claim 5, Kim has a substrate (100) on which the gate line (130a) is located, a gate insulating layer (120) on an entire surface of the substrate (100) including the gate line (130a), an amorphous silicon active region (110) on the gate insulating layer (120) above the gate line (130a), source (150) and drain (170) electrodes located at opposite sides of the amorphous silicon active region (110), a passivation film (160) formed on the entire surface of the substrate (100) including the source (150) and drain (170) electrodes.

Claims 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US 6,580,473 B2) in view of Song et al. (US 5,886,757) and further in view of Ono et al. (US 5,760,854).

As to claims 8 (amended)-12, Applicant's recited method steps of forming thin film transistors each having a gate electrode, a source electrode, and a drain on an insulating substrate, forming a passivation film on an entire surface of the substrate including the thin film transistors, forming a contact hole over a predetermined portion of the drain electrode and a pixel region adjacent to the drain electrode, and forming a pixel electrode in the pixel region connected to the drain electrode through the contact hole and *wherein the pixel electrode directly contacts the substrate* would have been obvious to one of ordinary skill in the art of liquid crystals at the time the invention was made in view of the device as taught and disclosed in the above noted references.

Response to Arguments

Applicant's arguments with respect to claims 1, 3 and 8 have been considered but are moot in view of the new ground(s) of rejection.

Because Applicant has not addressed the substantive rejections with regard to the dependent claims, Applicant is presumed to have acquiesced to the rejections of record regarding the dependent claims.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeanne A. Di Grazio whose telephone number is (571)272-2289. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim, can be reached on (571)272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeanne Andrea Di Grazio
Patent Examiner
Art Unit 2871

JDG

TARIFUR R. CHOWDHURY
PRIMARY EXAMINER